A High-Performance, Low-Cost Analog Switch Family

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Introduction

Siliconix' popular DG201 quad analog switch has been an industry workhorse for over two decades. To meet the demands of new applications for more precision and faster switching speeds, an improved version of the DG201, along with five other general purpose analog switches, is being introduced by Siliconix. The new "B" series provides lower switch on-resistance, leakage current, turn-on time, charge injection, and power consumption at prices comparable to industry-standard devices.

Behind these improved levels of performance is Siliconix' new high-voltage silicon gate process, HVSG-II. HVSG-II substantially increases the switch's overall performance, allowing analog signals to be switched efficiently from 20 V to +3 V. Even though these devices were designed on a high-voltage process, they still exhibit very good low-voltage performance and provide a single-supply solution.

These general-purpose parts are ideal for a host of applications, including automatic test equipment, instrumentation, and voice or data communications. This note details performance improvements, and provides a competitive comparison and overview of general applications.

Improved Single-Supply Operation

The "B" family can be used with split supplies or a single supply. The DG201B/202B have an internal +5-V regulator. The DG211B and DG212B are ideal for low-voltage single supply operation (+3 V to +5 V).

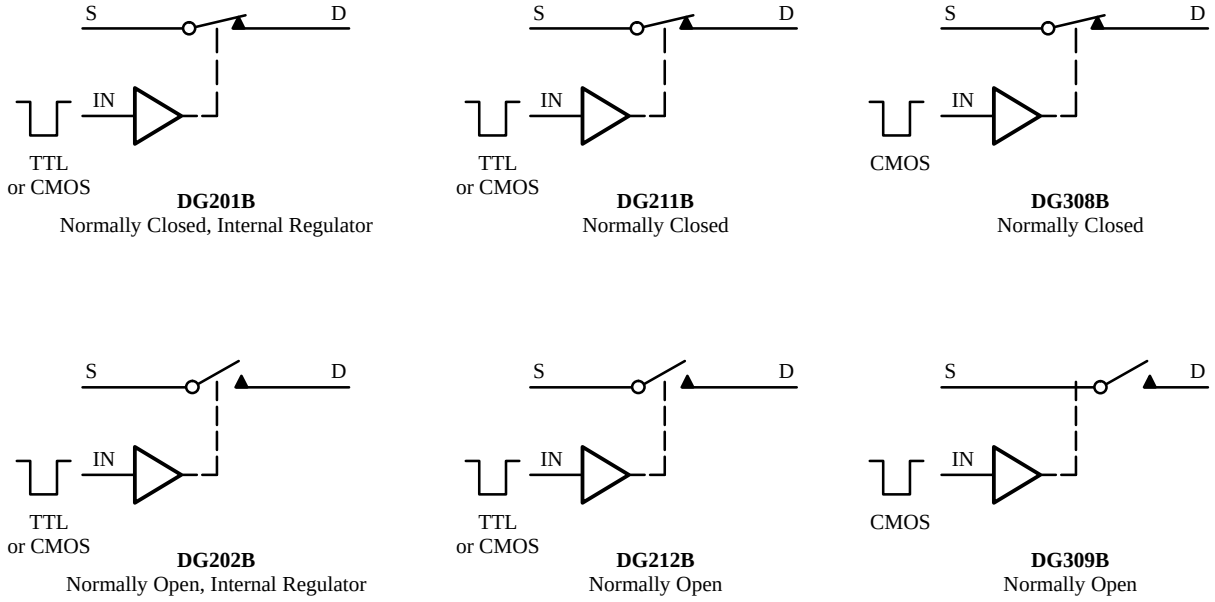


Figure 1. "B" Series Diagrams

Table 1. DG211B/212B Typical Low-Voltage Performance

V+ & V_L (V)	Logic Threshold (V)	t_{ON} (ns)	t_{OFF} (ns)
+5	+2.2	200	50
+4.5	+2	200	50
+4	+1.9	300	50
+3.3	+1.6	400	100
+3	+1.5	500	100
+2.5	+1.2	900	200
+2	+1	1600	400

Note: V_S = +2 V, R_L =1 kΩ, V– = 0 V

Simply connect V_L to V+ (Figure 2). The voltage at V_L sets the logic threshold (Table 1).

Even though the DG211B and DG212B operate as low as +2 V, their turn-on time increases proportionally to the decrease in V+. At +3.3 V these devices are quite suitable for general applications, even though their on-resistance can approach 1 kΩ. Later it will be shown how this resistance can also be substantially reduced. The DG201B/202B parts also were tested to < +3 V with similar performance (except t_{ON} which was slightly slower).

Speed Combined With Power

Normally the speed of an analog switch can only be increased at the expense of the power driving the chip. But the "B" series devices overcome this problem with reduced channel lengths and parasitic capacitances.

These improvements allow the DG211B's turn-on (t_{ON}) time to be reduced to 120 ns typical, and power dissipation (P_D) to be as low as 0.7 nW during the quiescent condition. Note that both t_{ON} and P_D are a function of the power supplies used to power the chip.

Table 1 shows the correlation between low voltage effects of the supply voltage used. The switching speed is typically 120 ns with split 15-V supplies. It slows to 1600 ns with a mere +2-V single supply. Turn-on time (t_{ON}) is measured from 50% of the INPUT logic control to 90% of the analog output signal. This interval includes the delay through the logic translator, FET driver stages, and the FETs themselves. An RC time constant comprised of the channel on-resistance and the output load capacitance (C_L) increases t_{ON} with an increase in C_L. This effect is minimal as long as a shunt resistive load is also present. The increase in t_{ON} is approximately equal to:

$$\Delta t_{ON} = r_{DS(on)} \times C_L$$

where C_L is the value above 35 pF (and 35 pF is the standard C_L used to measure t_{ON}).

Low On-Resistance

On-resistance can make a critical addition to the error budget in precision applications. For the "B" devices, typical $r_{DS(on)}$ is 45 Ω and is in series with a load resistance R_L (Figure 2). The error is equal to

$$r_{DS(on)}/(r_{DS(on)} + R_L) \text{ or } 45/(45 + 1\text{ k}) = 4.3\%$$

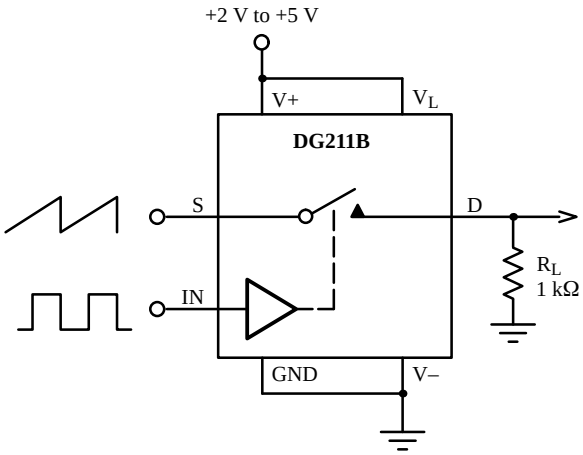


Figure 2. DG211B Single-Supply Operation

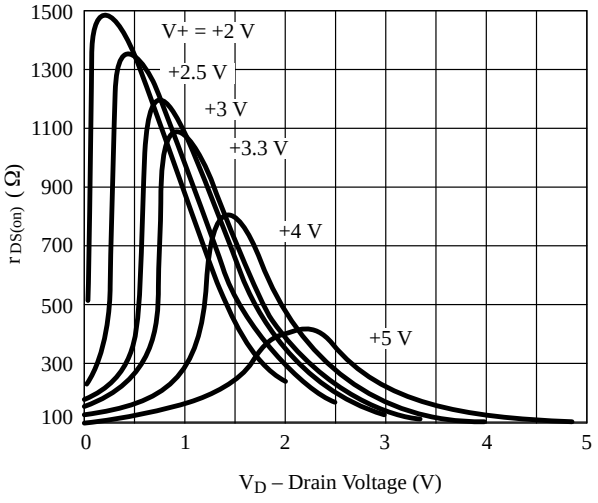


Figure 3. Low Voltage $r_{DS(on)}$ Curves

Increasing R_L will proportionally reduce this error. However, a large load resistance reduces the off-isolation. If the analog signal is dc, off-isolation is not a problem since it will not be coupled through the off-channel parasitic capacitor. But if the analog signal is ac, then the off-isolation decreases as the frequency increases or if R_L increases. One solution to this problem is to run the switch into the virtual ground of an inverting amplifier, as described below.

On-Resistance Flatness

On-resistance flatness is a measure of the change in $r_{DS(on)}$ when the source or drain voltage varies. This delta can distort the input signal as follows:

$$\text{Harmonic Distortion} = 20 \log \frac{\Delta R_{ON}}{R_L}$$

Limiting analog signal dynamic range to the flattest part of the $r_{DS(on)}$ curve can reduce this error. A "virtual ground" at the summing junction of an op amp can provide the high impedance required to reduce distortion. If the non-inverting input of an op amp is referenced to ground, a virtual ground appears at the inverting input because the input offset voltage (V_{OS}) of most op amps is in the microvolt or millivolt range. Thus the inverting input is only the value of this input voltage above or below ground. This virtual ground node is also a very high impedance point because

$$R_{IN} = \frac{V_{OS}}{I_B}$$

where I_B is the input bias current of the op amp. For instance, a typical op amp with V_{OS} = 1 mV and I_B = 1 nA would have an input impedance of 1 MΩ.

Bandwidth Improvements

The bandwidth of a general-purpose analog switch is generally not specified on most data sheets. Bandwidth can be calculated by this expression:

$$f_{-3db} = \frac{1}{2\pi RC}$$

where R = $r_{DS(on)}$ and C = $C_{D(on)}$, also R_L assumed to be infinite.

Substituting 45 Ω and 16 pF, respectively, results in a theoretical calculated bandwidth of ≈220 MHz. In reality, the switch has no real off-isolation at this frequency so the usable bandwidth is really a function of off-isolation. Since off-isolation is 60 dB at 3 MHz, then 3 MHz becomes the maximum usable frequency (assuming that 60 dB is the minimum acceptable limit). This relationship can be seen on the data sheet off isolation vs. frequency curve. At a bandwidth of 1 MHz, the off-isolation is 90 dB.

Bandwidth is also associated with insertion loss. This specification is expressed in dB and equals

$$20 \text{ Log } \frac{R_L + R_{ON}}{R_{ON}}$$

The insertion loss of the "B" series devices is generally 6 dB over the usable frequency range from 0 to 3 MHz with R_L = 50 Ω.

Charge Injection

Charge injection consists of the charge (measured in pC) transferred from the digital driver to the analog channel at the time of switching the device to the "off" state. This unwanted charge is normally induced through parasitic gate-to-source or gate-to-drain capacitances. In a sample-and-hold circuit, charge injection will cause an offset error called "hold-step." "B" series switches have glitch suppression circuitry on-chip and fewer parasitics at the gate. These improvements have reduced the typical charge to 1 pC, compared with the industry-standard specification of 20 pC.

Tips for reducing charge injection effects

Using the drain instead of the source for the output results in less glitch, but the "step" is slightly greater. This approach, however, isn't without its problems. The logic signal (IN) can be injected into the analog output path by the package interlead capacitance (pin-to-pin) which is generally about 0.75 pF. Another 1-3 pF is usually associated with the PC board stray capacitance, if the INPUT and DRAIN, which are adjacent to each other at the package, are laid out without a ground plane separation. The board used for this test measured about 3 pF of stray capacitance. Because of this interlead and board capacitance ("C_{stray}"), it is also recommended that the logic amplitude be clamped to about +3 V . The charge current is expressed here:

$$I = C \times \frac{dv}{dt}$$

where dv is the instantaneous logic voltage change and C is C_{stray}.

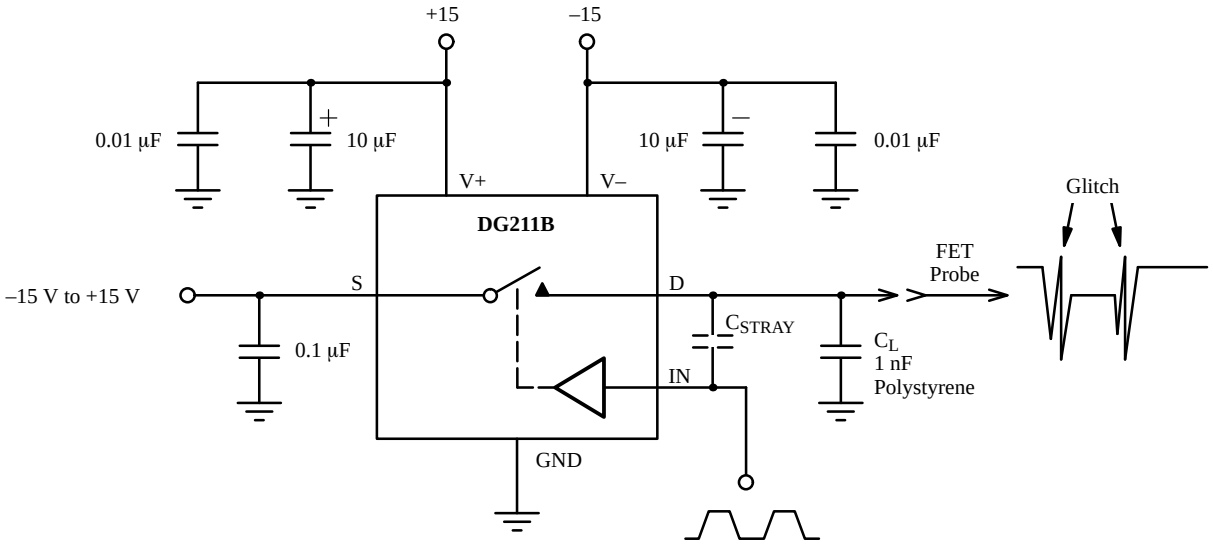


Figure 4. Charge Injection Test Circuit

Charge current (I) can be reduced if dv is reduced, where dv is the logic control signal amplitude. Note, for example, the reduction of current injected into the hold capacitor (C_L) shown in Figure 4. A proper ground plane separation or guard, as well as logic clamping, can substantially reduce the charge injection caused by C_{stray}. A single point ground (with digital and analog grounds separated), or a ground plane, should be used to reduce ground loops and switching noise. Figure 6a depicts the "B" series actual hold-step of 9 mV with +2 V at the source. Maxim's best currently available equivalent device, for example, offers a 14-mV hold-step (Figure 6b) measured at turn-off. To achieve a Q of 1 pC (which is actually 1 mV) using a "B" series device, the voltage at the source should be at ground and the logic amplitude clamped to about +3 V. Or reduce Cstray. The voltage change can be calculated by:

$$\Delta V = \frac{Q}{C_L}$$

A 10-Ω damping resistor in series with the hold capacitor (Figure 5), actually increases the effects of charge injection. The load becomes more resistive. C_L could be increased to about 10 nF, which would help suppress the glitch and hold-step (while decreasing the droop rate in S/H circuits).

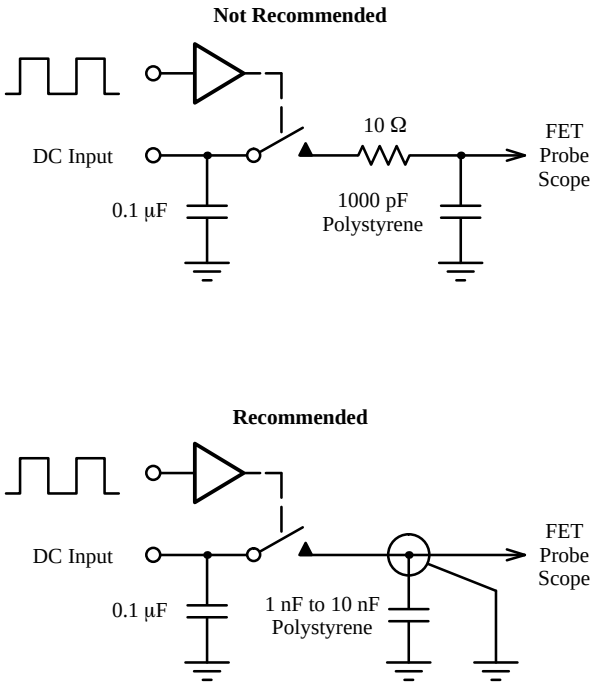


Figure 5. Reducing Charge Injection Effects

Faster Turn-on Times

In the new "B" series, t_{ON} has been reduced from 480 ns to 120 ns. Maxim's best currently available equivalent device, by comparison, has both a slower t_{ON} and a glitch with a very slow recovery time (Figure 6b). Parts like this need a 1.0-µs de-glitcher to make them usable. Of course, this "solution" also adds to the cost of implementation. The "B" series parts require only 300 ns to settle out (Figure 6a).

Improved On-Resistance and Leakage Current

While C_L can be increased to reduce glitch, this approach can be a problem in sample-and-hold circuits. There is a trade-off between acquisition time and droop-rate. An increase in C_L slows the droop-rate but increases the acquisition time. The droop-rate can be understood as the voltage change caused by the sum of

- the drain-off leakage current ($I_{D(off)}$),
- the capacitor leakage (I_C), which is caused by the dielectric absorption of the capacitor, and
- the bias current (I_B) if a buffer amplifier is used after the hold capacitor C_L.

or,

$$\frac{dv}{dt} = \frac{I_{D(off)} + I_B + I_C}{C_L}$$

For the "B" series, typical leakage current at room temperature has been improved from 20 pA to only 10 pA.

On-resistance and leakage are critical in determining circuit accuracy. Drain-on leakage for "B" series devices has been reduced to 20 pA from the industry-standard 150 pA. This current directly increases the error or voltage drop across the channel. This error increases the circuit offset voltage. The error is calculated by:

$$V_{error} = r_{DS(on)} \times I_{D(on)}$$

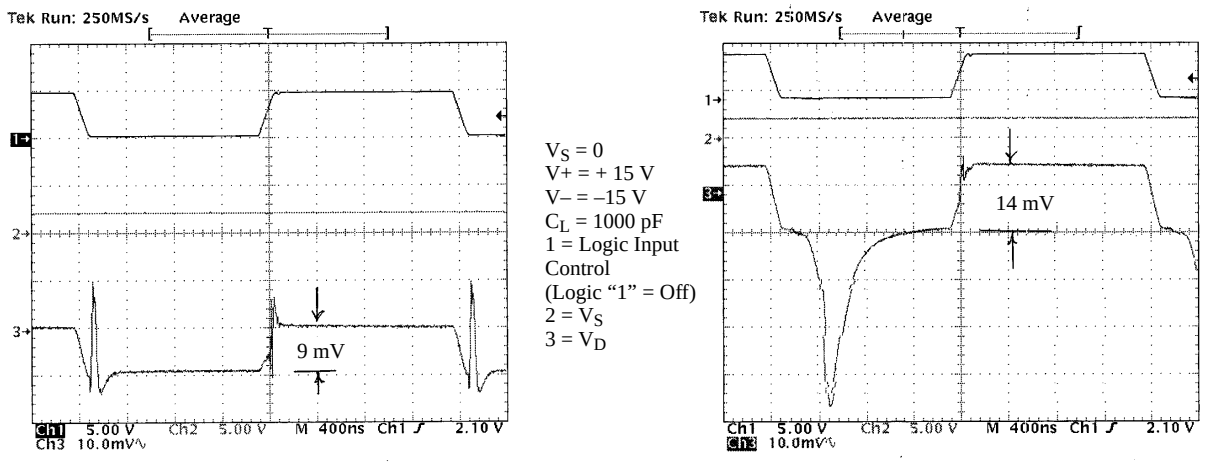
For the "B" series parts, on-resistance is substantially reduced from 115 Ω to 45 Ω, which also reduces the above error.

Power Consumption

The power dissipated by the DG211/212B devices has been reduced to <1 nW typical. Competing devices range from 400 nW to 18 mW. The combination of high speed and low power consumption is a unique feature of the new "B" series. Power consumption is equal to

$$(V+)(I+) + (V-)(I-) + (V_L)(I_L)$$

which is a quiescent condition calculation. This can be added to the channel power when the switch is in a dynamic state. The power consumed by the analog channel is determined by I^2R where (I) is the current through the channel and (R) is $r_{DS(on)}$.



a) DG201B Glitch and Hold Step due to Charge Injection

b) Competitor M's DG201A Glitch and Hold Step

Figure 6.

General Applications

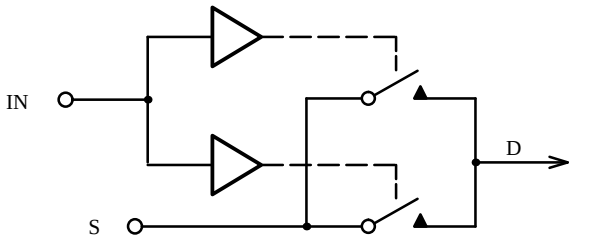
The “B” series general-purpose switches are recommended for ATE, instrumentation, communications, and other applications requiring analog signal processing. Analog switches can be used just like passive components. For instance, general uses include switches in parallel, switches in series, switches in “inverted L,” and switches in “T” configurations.

Two or more switches can be used in parallel by simply connecting source-to-source, drain-to-drain, and input-to-input (Figure 7a). This configuration proportionally increases maximum channel current and reduces on-resistance. For instance, two switches in parallel double the maximum channel current and cut $r_{DS(on)}$ in half.

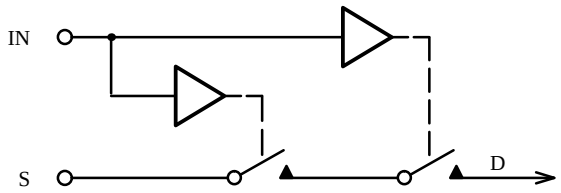
Switches in series are sometimes used to increase off-isolation (Figure 7b). This approach has a price, however, since on-resistance doubles. A better way to increase off-isolation is the “inverted L” circuit (Figure 7c). When the series switch turns off, the shunt switch turns on and clamps the analog signal to ground. This substantially reduces the chance of any signal passing through to the switch output. The ultimate isolation is provided by a “T” switch (Figure 7d). This configuration is useful when the application calls for a high degree of isolation without grounding the switch input or output.

The “B” series does not include NO and NC switches in the same package, but an SPDT circuit can still be easily configured using three SPST switches (Figure 8). One switch is used as a logic inverter that converts a NO switch to a NC switch. Then, with NO and NC switches, the sources can be connected to form a pole with a double-throw output at the drains. Note that the 10-kΩ pull-down resistor will slow the turn-off time to about 800 ns.

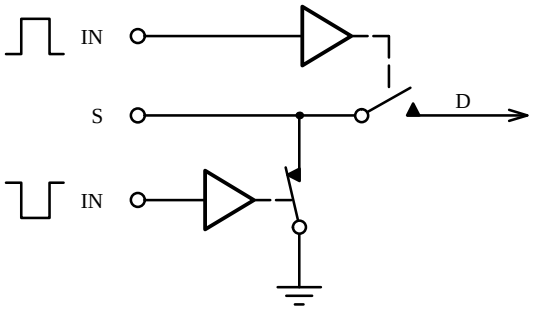
Many of today’s applications call for precision single-supply analog switches. The circuit in Figure 9 shows a typical inverting op amp circuit with $A_V = –1$. The summing junction (or “virtual ground,” if the amplifier is referenced to ground) is a high Z point. As noted above, the ratio $\Delta r_{DS(on)}/R_L$ can reduce harmonic distortion. If the drain of S1 sees this high Z when the switch is closed, distortion is substantially reduced. Since the voltage at the summing junction is constant, $r_{DS(on)}$ modulation is eliminated. Since this summing point is also at a virtual +2 V (or virtual ground when referenced to ground), it increases the off-isolation.



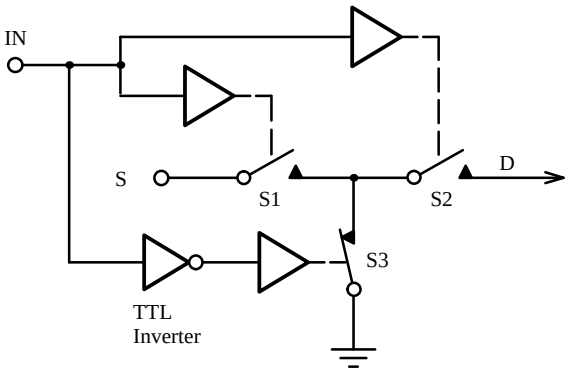
a) Parallel Switches



b) Series Switches



c) Inverted “L” Switches



d) “T” Switches

Figure 7. General Applications

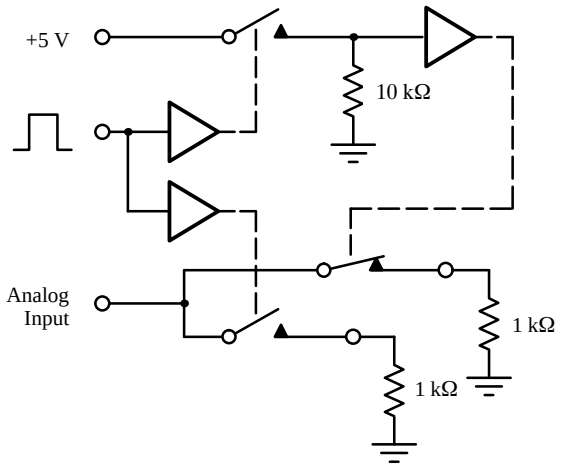


Figure 8. Design SPDT Switch with 3 SPST

S2 is used for temperature compensation and tracks the $r_{DS(on)}$ of S1 to minimize gain error. Note that S2 is always closed, to avoid disturbing the op amp when S1 opens. The op amp remains closed loop. The reference is set at +2 V to establish a +3-V output offset . The input signal swings 2 Vp-p and is offset by +1 V. It was necessary to raise the virtual ground and ensure the amplifier doesn't distort or clip the signal. It is critical that S1 be placed right at the summing point. For instance, if S1 is placed on the other side of the input resistor, that resistor value would set R_L instead of the high Z of the summing point. Also, R_{ON} would change, causing distortion.

Conclusion

The Siliconix "B" series of analog switches offers a high-performance, low-cost solution to many of today's analog signal processing applications. The new "B" family has substantially improved the key parameters—$r_{DS(on)}$, $I_{D(ON)}$, t_{ON}, P_D, and Q—without increasing the price. These new switches are also ideal for many high-speed, high precision, single-supply analog circuit functions. Many existing designs can improve circuit performance by simply upgrading to the equivalent "B" family device. The improved parameters provide the six key benefits that designers look for:

- less signal loss
- higher accuracy
- higher sample rates
- faster settling times
- fewer transients
- power savings.

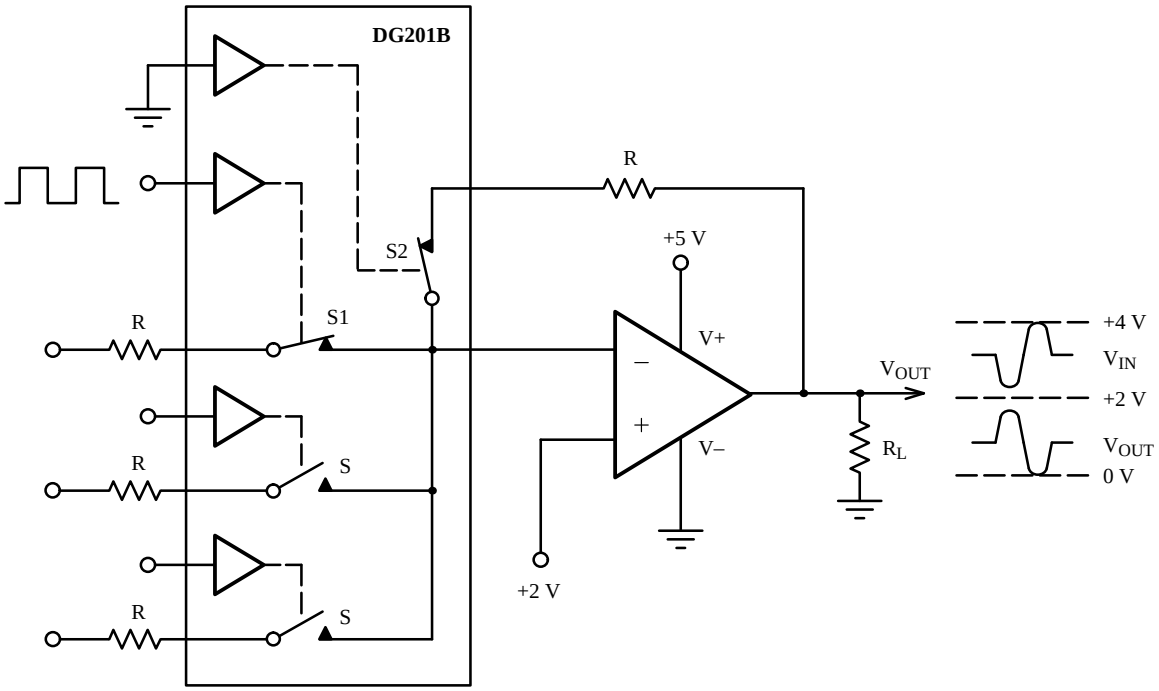


Figure 9. DG201B Single Supply and Summing Point (A Low Distortion Single Supply Summing Amplifier)